REMARKS

I. Status of Claims

Claims 1, 4-8, 10 and 14-16 are pending.

Claims 1, 4-8, 10 and 14-16 stand rejected.

Claims 2, 12-13 were cancelled in a prior response.

Claims 1, 4-8, 10 and 14-16 have been cancelled herein.

Claims 17 – 23 are new claims.

III. Objection to the Claims

The examiner has objected to claims 4, 5, 10 and 16 for containing informalities. Applicant, through his attorney, again wishes to thank the examiner for his observations and has made new claims which include corrections to the noted informalities.

Having made new claims to correct the informalities, applicant submits that the reasons for the examiner's objection to the claims have been overcome and can no longer be sustained. Applicant respectfully requests that the objection be withdrawn.

IV. Rejection pursuant to 35 USC §112 First Paragraph

The examiner has rejected claims 1, 4-8, 10 and 14-16 pursuant to 35 USC §112, first paragraph because "in each of the independent claims, applicant claims that the burst transfers are accomplished '*independent of a count (number) of words to be exchanged* (transferred)' between the first and second processors," and that "the main processor[] would have to inherently know how many data words it needs to transfer." (emphasis added). The applicant has not included this phrase in new independent claims, which contain the phrase "without receiving a data word count or stop address." Support for this limitation appears in the specification at page 5, lines 5 – 9.

Applicant respectfully requests the rejection be withdrawn and the new claims allowed.

V. Rejection pursuant to 35 USC §112 Second Paragraph

The examiner has rejected claim 1 for insufficient antecedent basis for the limitation of "said identified block." The applicant has cancelled all claims referring to memory blocks and respectfully requests that this rejection be withdrawn and the new claims allowed.

V. Rejection pursuant to 35 USC §103

The examiner has rejected claims 1, 4, 6-8 and 16 as being anticipated by Campanini U.S. Patent No. 4,700,292 (Campanini or '292) and claims 5, 10 and 14-16 as being anticipated by Campanini in view of U.S. Patent No. 5,109,49 (Armilli or '490).

The applicant has cancelled these claims and submits herewith new claims that overcome the rejections based on Campanini. New independent claim 17 recites "(a) a first processor having one address bus, one data bus, control signals and memory accessible via the address bus and data bus; (b) a second processor coupled directly to the address bus, data bus and control signals of said first processor." The specification supports this, as shown in applicant's Figure 1, with Processor 110 directly connected to the interface components (121, 122 and 123) of co-processor 120.

The prior art of record neither discloses nor suggests "a first processor having one address bus, one data bus, control signals and memory accessible via the address bus and data bus [and] a second processor *coupled directly to the address bus, data bus and control signals* of said first processor." Instead, the reference (Campanini) shows a two-processor system wherein the processors each have their own internal address and data buses as well as interface hardware for communications over yet a third bus.

Referring to Figure 1 in Campanini, both central processing units (CPU_A and CPU_B) communicate over their individual internal buses (B_A and B_B) with a dedicated interface (INT_A and INT_B). The interfaces are what connect the dual processors over yet a third bus (B_C).

Unlike the topography in Campanini, which requires inter-processor communication over a dedicated bus (B_C), the claim 17 requires "A dual processor system, comprising: (a) a first processor having *one* address bus, *one* data bus, control signals and memory accessible via the address bus and data bus; (b) a second processor *coupled directly to the address bus, data bus*

and control signals of said first processor." (Claim 17). See also Claim 20: "A multi-processor system, comprising: (a) a first processor having *one* address bus, *one* data bus, control signals and memory accessible via the address bus and data bus; (b) at least one *next processor coupled directly to the address bus, data bus and control signals of said first processor*" and Claim 22: "A coprocessor comprising: a control register with a control register system address, an internal memory, a data register having a data register system address and coupled to the internal memory, and an internal address generator coupled to the control register and to the internal memory, wherein: a master processor, having *one* address bus, *one* data bus, control signals and memory accessible via the address bus and data bus, can be coupled to said coprocessor with at least one of the signals of the address bus coupled directly to the coprocessor control register and the *first processor data bus coupled directly to the coprocessor data register* and to the coprocessor control register."

In addition, Campanini requires that both processors have dedicated interface hardware for communication with the other processor (Campanini, Fig. 1 INT_A and INT_B). Unlike Campanini, claim 17 covers a system wherein the "second processor [is] *coupled directly to the address bus, data bus and control signals of said first processor.*" Accordingly, the applicant has cancelled all claims to which the examiner has objected on the basis of Campanini and submits new claims 17 – 23. Applicant respectfully suggests that the new claims overcome the examiner's rejection based on Campanini and requests that the rejection be withdrawn and the new claims allowed.

VIII. Conclusion

Having addressed the examiner's rejections, applicant submits that the reasons for the examiner's rejections have been overcome by the new claims and remarks made herein, and the rejections can no longer be sustained. Applicant respectfully requests reconsideration and withdrawal of the rejections and that a Notice of Allowance be issued.

Should any unresolved issues remain, the examiner is requested to call Applicant's attorney at the telephone number below.

The Commissioner for Patents is hereby authorized to charge any fees or credit any excess payment that may be associated with this communication to Duane Morris LLP deposit account 50-2061.

Respectfully submitted,

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